

**Novel Stacking Process:** Sony researchers will show how a successful electrical connection through three layers can be achieved, paving the way toward a process for three-layer stacked 3D heterogeneous integration. They will describe a chip-on-wafer-on-wafer (CoWoW) process, involving a three-layer vertically stacked structure comprising face-to-back (F2B), chip-on-wafer (CoW), and face-to-face (F2F) wafer-on-wafer (WoW) using 6 µm-pitch copper-to-copper (Cu-Cu) connections. Bowing of the top chip was controlled to achieve void-free CoW bonding, and CoW bonding strength was simulated using elastic strain energy testing. Excellent 6 µm-pitch Cu-Cu connections of F2B CoW were achieved, both at the center and at the edge of the chip, as well as F2F WoW.

Additionally, the 6 µm-pitch Cu-Cu connections using CoWoW exhibited high reliability in stress-induced voiding (shown above) and electromigration tests.

**(Paper #2.4, “*Novel Three-Layer Stacking Process with Face-to-Back CoW 6 µm-Pitch Hybrid Bonding*,” A. Urata et al, Sony)**